USB hub / host

USB 5V

LDO
( 1.8 V / 2.5 V / 3.3 V )
Through Jumper Selection

USB (D+ and D-)

CLK_SE (Clock Single-Ended)

SMA

VDD_DUT
*(DUT: Design Under Test)*

I2C Pull-Up Resistors

CY8C5868LTI-LP039 (PSoC 5LP)

I2C lines : SCL, SDA

CY29430 FLQXI

CLK_P

CLK_N

Termination Settings

SMA

SMA

Vc

VCXO input

FS Jumper
*(FS: Frequency Select)*

FS1_DUT

FS0_DUT

OE Control Jumper
*(OE: Output Enable)*

OE

XIN

XOUT

Crystal

LED Indicators

(1) PSoC 5LP enumeration (Green)
(2) CY29430 Power (Amber)

SMA

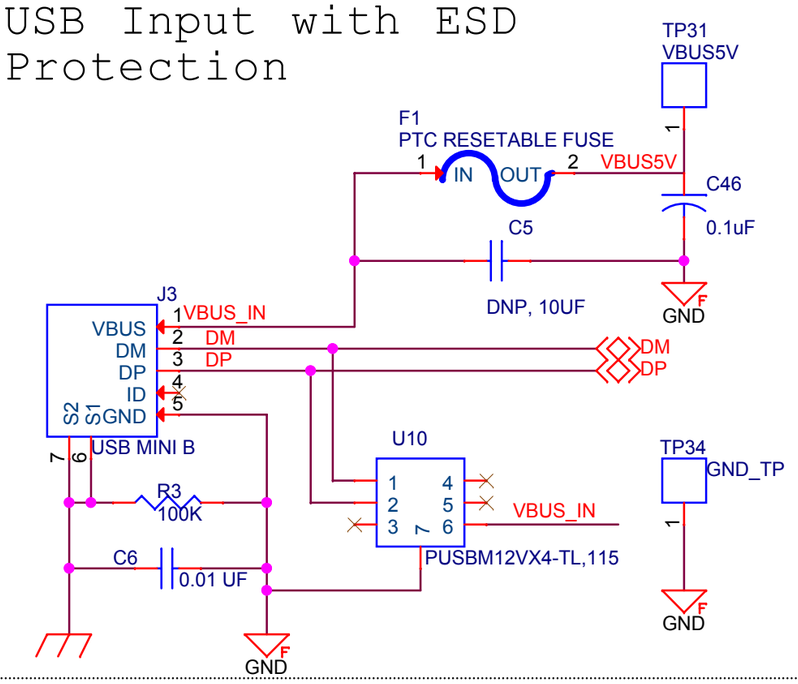
TCXO input

zero ohm

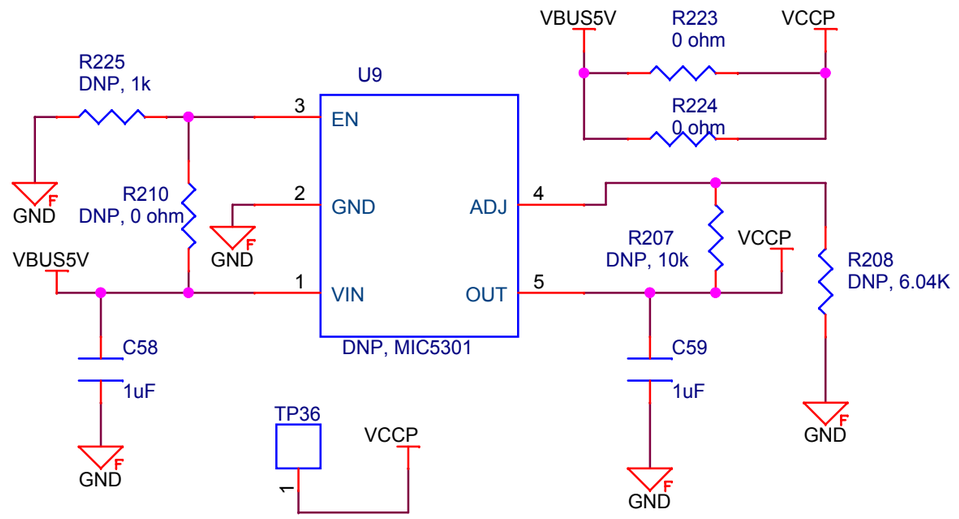
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| | | |
|---|---|---|
| Title: **Block Diagram of CY3677 Evaluation Kit** | | |
| Size: A4 | Document Number: **630-60313-01** | Rev: **02** |
| Date: Thursday, December 15, 2016 | Sheet 1 of 4 | |

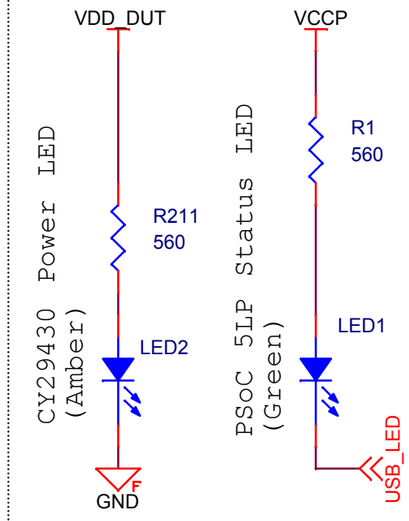
## USB Input with ESD Protection



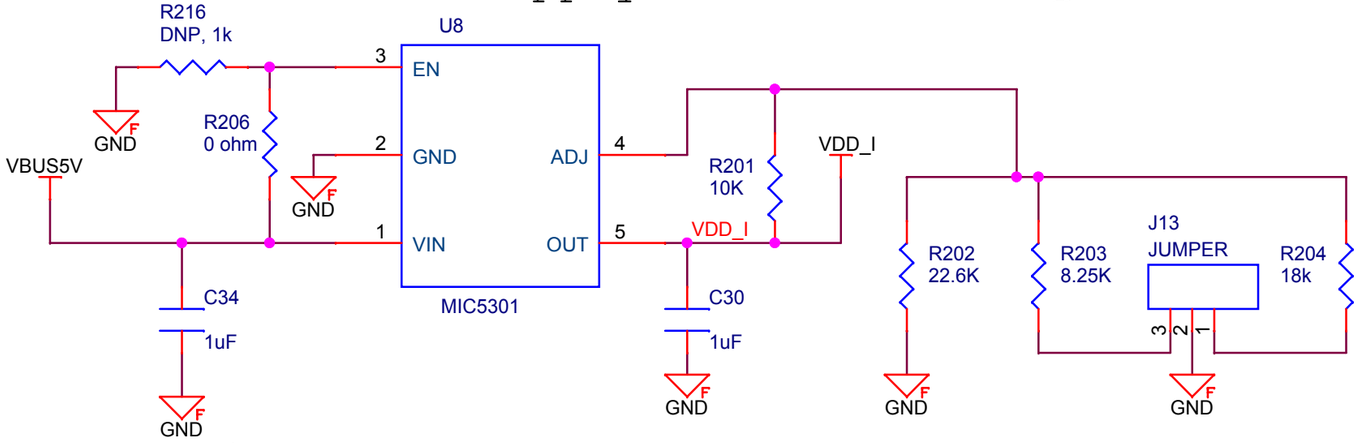

## LDO Supply for PSoC 5LP




## Power and Status LEDs




## LDO Supply for CY29430FLQXI




Default J13 setting:
Jumper shunt populated between pin 2 & 3

**Note: The J13 jumper setting should match the Vdd profile created in the ClockWizard. Refer the following Table to set the supply voltage of U1.**

| Jumper (J13) settings | VDD_I |
|---|---|
| Short 2 & 3 | 3.3V |
| Short 1 & 2 | 2.5V |
| Open | 1.8V |

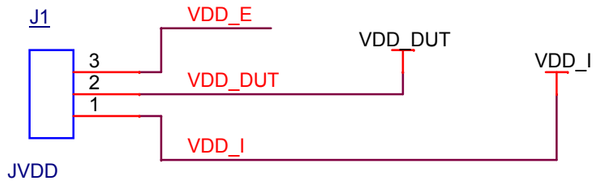
Layout :Include this Table on the silk-screen top

Calculation :

VREF = 1.25 V
Vout (i.e. "VDD_I") = VREF X ( 1 + R201 / Reff )

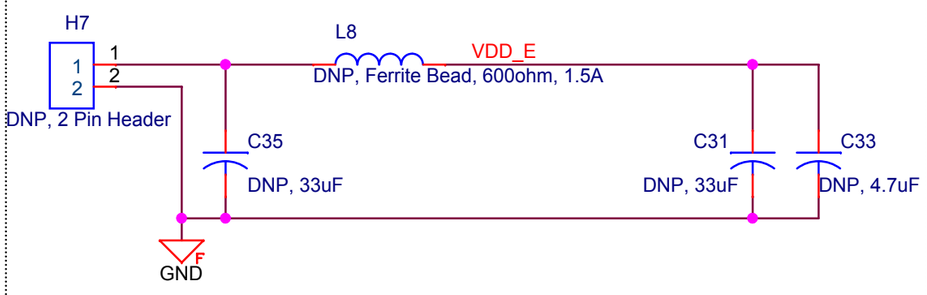
Reff = R202 : J13 open
= ( R202 || R203 ) : J13 short 2 and 3
= ( R202 || R204 ) : J13 short 2 and 1

## Supply Jumper




Default :
Jumper shunt populated between pin 1 & 2

## Debug Point for CY29430



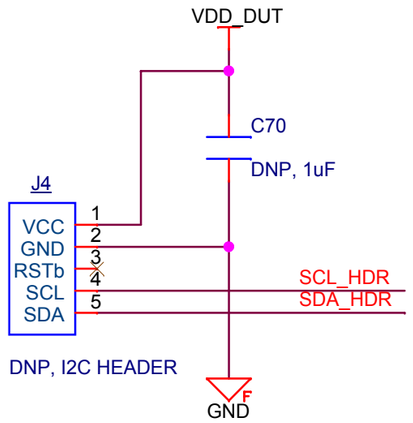

PCA : 121-60312-01 Rev 03
PCB : 600-60335-01 Rev 02
FAB DRW : 610-60307-01 Rev 02
ASSY DRW : 620-60315-01 Rev 02

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| | | |
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| Date: Monday, December 12, 2016 | Sheet 2 of 4 | |

# PSoC 5LP Connections

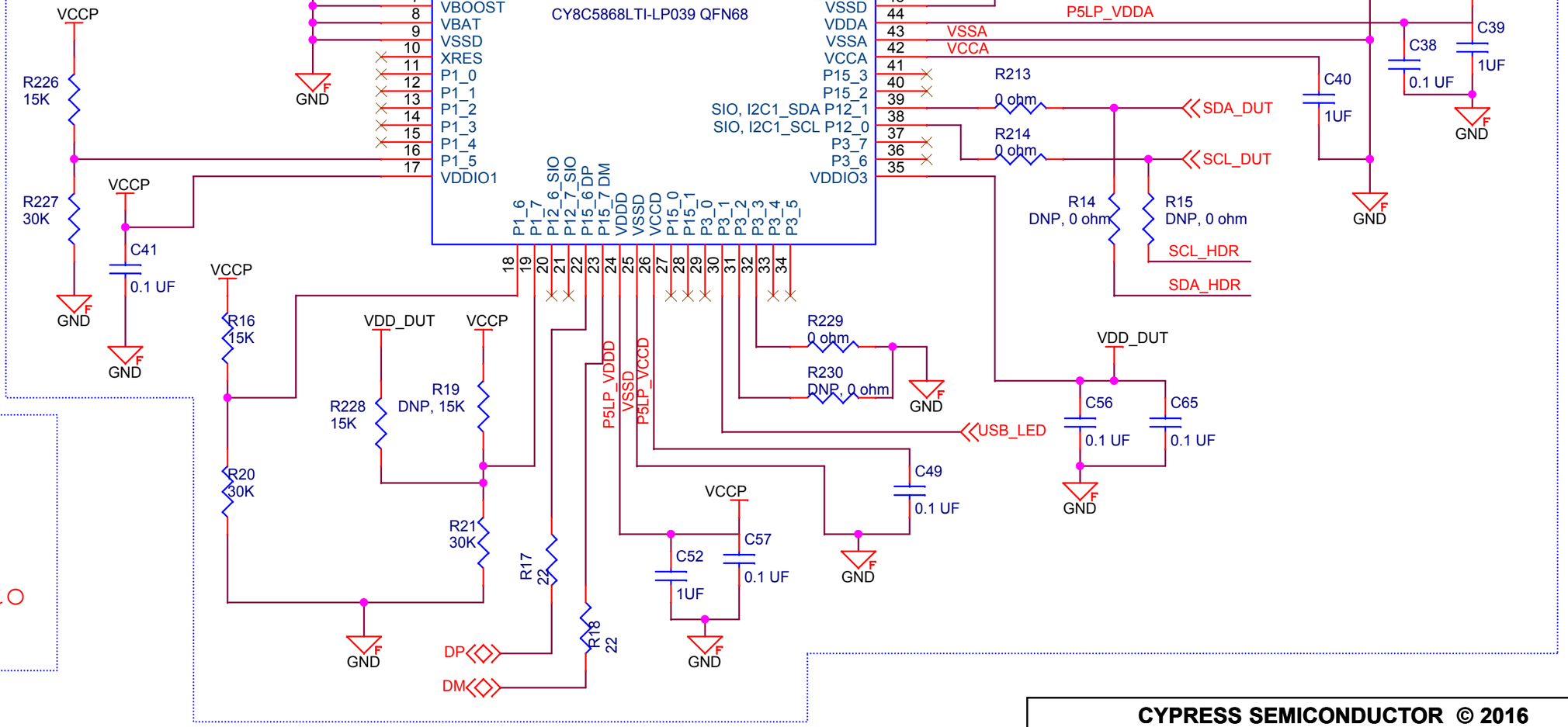
## 5-Pin I2C Header




J4 is DNP




Layout : (1) C67 to place close to pin U7.44, (2) C66, C68 to place close to pin U7.67

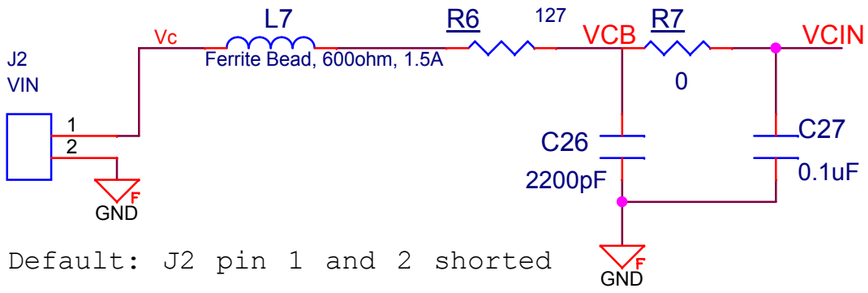



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PCB : 600-60335-01 Rev 02
FAB DRW : 610-60307-01 Rev 02
ASSY DRW : 620-60315-01 Rev 02

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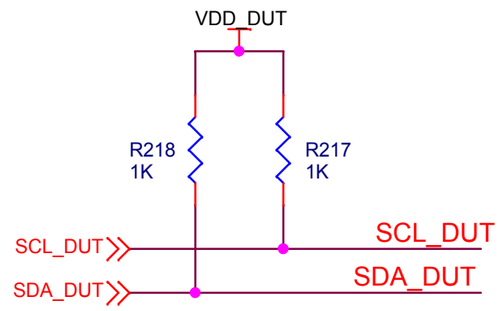
| | | |
|---|---|---|
| Title: CY3677 Evaluation Kit | | |
| Size: A4 | Document Number: 630-60313-01 | Rev: 02 |
| Date: Monday, December 12, 2016 | Sheet 3 of 4 | |

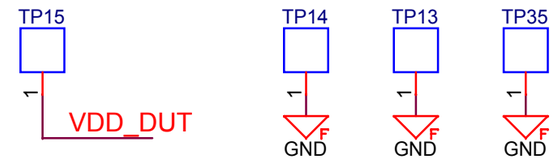
## Vcontrol Interface (VCXO)




Default: J2 pin 1 and 2 shorted

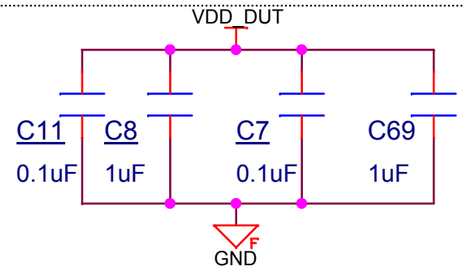
## I2C Pull up




Layout : Test Points Spread around U1

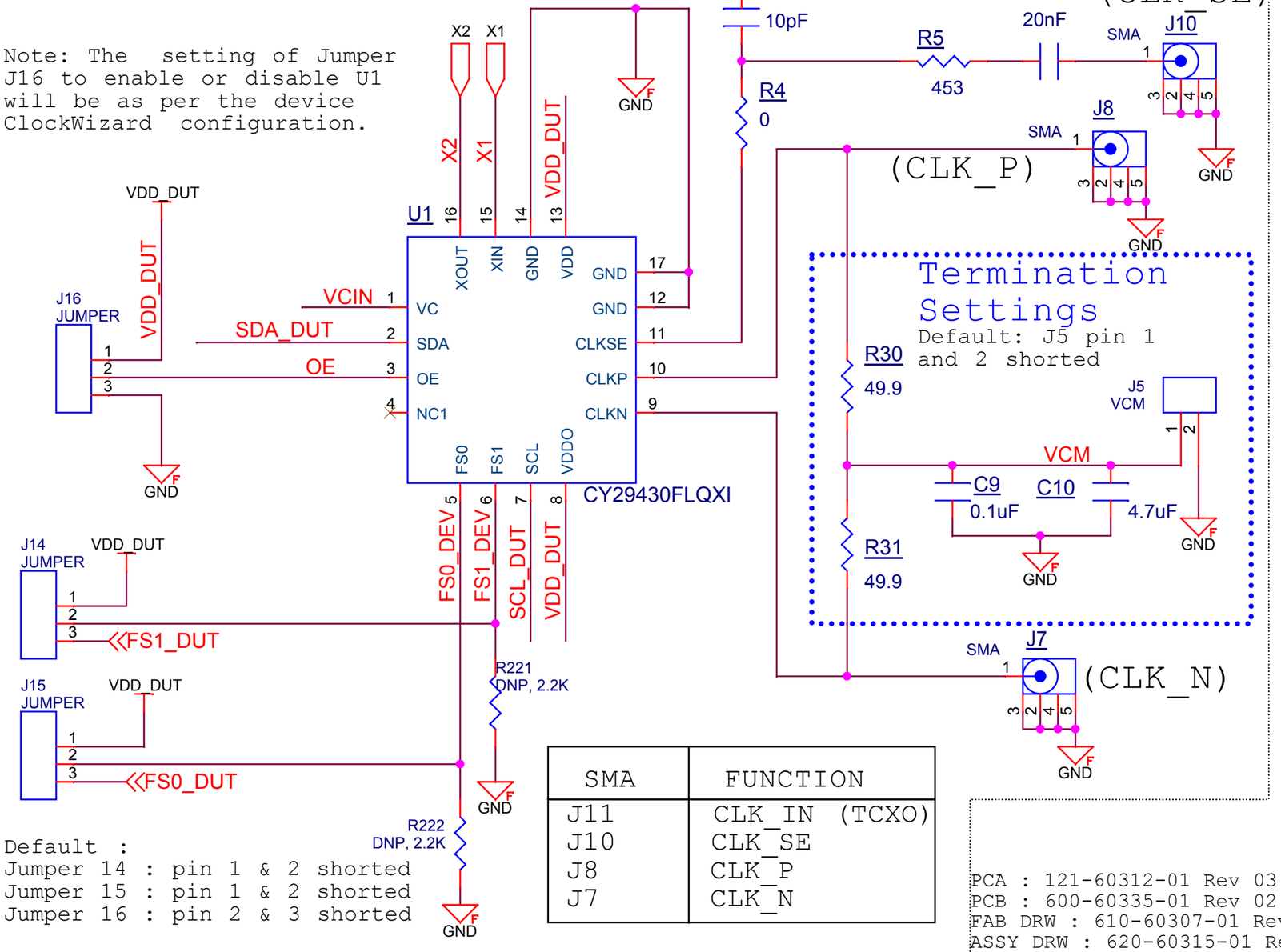
TP15, TP14, TP13, TP35 test points are DNP.




Layout : Decaps should be placed close to IC Supply and Ground pins

## CY29430FLQXI Interface

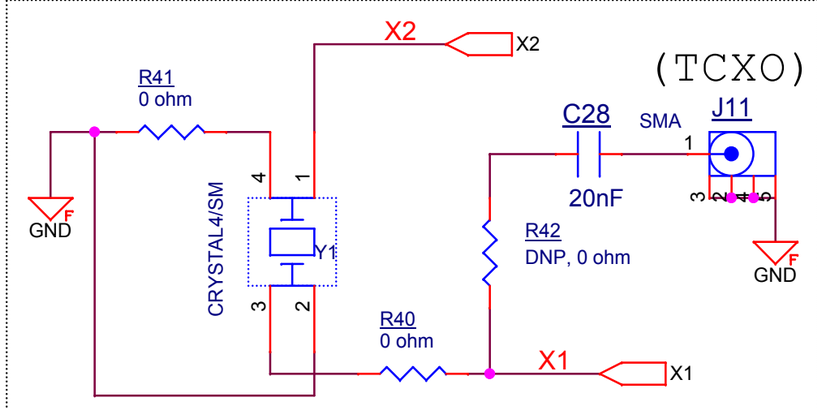
Note: The setting of Jumper J16 to enable or disable U1 will be as per the device ClockWizard configuration.




Default :
Jumper 14 : pin 1 & 2 shorted
Jumper 15 : pin 1 & 2 shorted
Jumper 16 : pin 2 & 3 shorted




| SMA | FUNCTION |
|---|---|
| J11 | CLK_IN (TCXO) |
| J10 | CLK_SE |
| J8 | CLK_P |
| J7 | CLK_N |




Layout : Crystals to be placed close to pin 15 and 16 of U1. Also the length of the traces X1, and X2 should as short as possible.

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ASSY DRW : 620-60315-01 Rev 02

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